Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

1. (*Currently Amended*) A method of mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising the steps of:

(1) defining a set of at least two possible pulses, each having a bit sequence corresponding to the same digital level, including at least two pulses having different time domain centroids;

(2) receiving at the input of the circuit a signal corresponding to said digital level and in response, selectively providing at the output of the circuit, as an output pulse, one and only one of said set of possible pulses corresponding to said digital level; and

(3) controlling step (2) such that over time a similar number of each of said pulses having different time domain centroids ~~are~~ is provided at the output of the circuit.

2. (*Previously Presented*) A method of mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising the steps of:

(1) defining at least first and second possible pulses, each having a bit sequence corresponding to the same digital level;

(2) receiving at the input of the circuit a signal corresponding to said digital level and in response, selectively providing at the output of the circuit, as an output pulse, one of said possible pulses corresponding to said digital level; and

(3) if said possible pulses corresponding to said digital level received at the input of the circuit have different time domain centroids, controlling step (2) to alternate between said first and second possible pulses each time said digital level is received.

3. (*Currently Amended*) A method of mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising the steps of:

(1) defining pulses for a plurality of digital levels to produce at least first and second pulse sets, each pulse set defining a bit sequence corresponding to each of said plurality of digital levels;

(2) receiving at the input of the circuit a signal corresponding to said digital level and in response, selectively providing at the output of the circuit, as an output pulse, one of said pulses defined in one of said first and second pulse sets; and

(3) if said possible pulses corresponding to said digital level received at the input of the circuit have different time domain centroids, controlling step (2) such that over time a similar number of each of said possible pulses ~~are~~ is provided at the output of the circuit to represent said digital level when said digital level occurs at the input of the circuit.

4. (*Currently Amended*) The method of claim 3, wherein in step (3), each time said digital level is received at the input of the circuit, the pulse set from which the output pulse is taken alternates, for at least those digital levels where said pulse sets have different pulses corresponding to said digital level[[,]].

5. (*Original*) The method of claim 3, wherein in step (3), said output pulses are selected from said first and second pulse sets by alternating between said first and second pulse sets, for at least those digital levels where said pulse sets have different pulses corresponding to said digital level.

6. (*Original*) The method of claim 5, wherein the pulses in each pulse set have similar time domain centroids, for at least those digital levels where said pulse sets have differing pulses corresponding to said digital level.

7. (*Currently Amended*) A method of mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising the steps of:

(1) defining at least first and second possible pulses, wherein said first and second possible pulses are pulse width modulated representations of said digital level;

(2) receiving at the input of the circuit a signal corresponding to said digital level and in response, selectively providing at the output of the

circuit, as an output pulse, one of said possible pulses corresponding to said digital level; and

(3) if said possible pulses corresponding to said digital level received at the input of the circuit have different time domain centroids, controlling step (2) such that over time a similar number of each of said possible pulses ~~are~~ is provided at the output of the circuit to represent said digital level when said digital level occurs at the input of the circuit.

8. (*Currently Amended*) A system for mapping a series of digital levels received at an input of a digital modulator circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least first and second possible pulses, each having a bit sequence corresponding to the same digital level;

pulse generation means for selectively generating one of said possible pulses corresponding to said digital level as an output pulse at the output of the digital modulator circuit; and

control means for controlling said pulse generation means such that when said possible pulses corresponding to said digital level are different, over time a similar number of each of said first and second possible pulses ~~are~~ is provided at the output of the digital modulator circuit.

9. (*Currently Amended*) A system for mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least first and second possible pulses, each having a bit sequence corresponding to the same digital level;

pulse generation means for selectively generating one of said possible pulses corresponding to said digital level as an output pulse at the output of the circuit; and

control means for controlling said pulse generation means such that when said possible pulses corresponding to said digital level are different, over time a similar number of each of said possible pulses ~~are~~ is provided at the output of the circuit, said control means including means for selectively providing one of said first and second pulses by alternating between said possible pulses each time said digital level is received.

10. (*Currently Amended*) A system for mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least first and second possible pulses, each having a bit sequence corresponding to the same digital level;

pulse generation means for selectively generating one of said possible pulses corresponding to said digital level as an output pulse at the output of the circuit; and

control means for controlling said pulse generation means such that when said possible pulses corresponding to said digital level are different, over time a similar number of each of said possible pulses ~~are~~ is provided at the output of the circuit,

wherein said mapping means further comprises means for defining at least first and second pulse sets, each pulse set defining a bit sequence corresponding to each of a plurality of digital levels.

11. (*Original*) The system of claim 10, wherein said control means further comprises means for alternating the pulse set from which the output pulse is taken each time said digital level is received at the input of the circuit, for at least those digital levels where said pulse sets have different pulses corresponding to said digital level.

12. (*Original*) The system of claim 10, wherein said control means further comprises means for selecting said output pulses from said first and second pulse sets by alternating between said first and second pulse sets, for at least those digital levels where said pulse sets have different pulses corresponding to said digital level.

13. (*Original*) The system of claim 12, wherein the pulses in each pulse set have similar time domain centroids, at least for those digital levels where said pulse sets have differing pulses corresponding to said digital level.

14. (*Currently Amended*) A system for mapping a series of digital levels received at an input of a circuit to a series of corresponding pulses at an output of the circuit, comprising:

mapping means for defining at least first and second possible pulses, each having a bit sequence corresponding to the same digital level;

pulse generation means for selectively generating one of said possible pulses corresponding to said digital level as an output pulse at the output of the circuit; and

control means for controlling said pulse generation means such that when said possible pulses corresponding to said digital level are different, over time a similar number of each of said possible pulses ~~are~~ is provided at the output of the circuit,

wherein said first and second possible pulses are pulse width modulated representations of said digital level.

15. (*Cancelled*)

16. (*Previously Presented*) The system of claim 8 wherein said digital modulator circuit is part of a cable television receiver.